Abstract-- This paper describes the architecture, the performance and the qualification tests of the Tracker detector power supply system for the AMS-02 experiment. The AMS-02 experiment will measure the cosmic ray spectrum from 0.5 GeV up to several TeV in space, looking for anti-matter, dark matter and strange quark matter. The experimental apparatus will be installed in the International Space Station (ISS) in year 2008. A preliminary version of this experiment has flown in 1998 on the STS-91 shuttle flight. The power supply system of the tracker has been designed optimizing noise performances, modularity and efficiency. Power is generated starting from a 28V line coming from the power distribution box for the entire experiment. This power is converted into the needed voltages by means of DC-DC converters, and for bias supply and front-end voltages is postregulated by means of linear regulators. Components Off The Shelf (COTS) have been extensively used in the construction of this power supply, however various radiation test campaigns have been performed in order to verify the reliability of these components. Active components were tested for total dose radiation damage and digital components were also tested for single event effects. The power supply architecture developed for the tracker detector has been used as a guideline for the development of the power supplies for the other detectors in the experiment.

I. INTRODUCTION

This paper describes the power supply system for the AMS-02 tracker detector which has been used as a reference for designing the various power supply system in the whole apparatus. The AMS experiment (Alpha Magnetic Spectrometer) has as physics goals the search for anti-nuclei, dark matter and strangelets, the measurement of the cosmic ray primary spectrum, the measurement of cosmic ray trapped component around 350 km of altitude and the observation of diffuse and source-emitted gamma rays. The instrument that will perform this measurement will take data on the International Space Station (ISS) starting from March 2008. A preliminary version of the AMS instrument (also known as AMS-01) has been flown on the Space Shuttle Discovery in June 1998 collecting a large set of experimental data (10^8 triggers) that helped the collaboration to validate the instrument and the analysis procedure and gave some interesting preliminary physics results [1].

The AMS instrument (fig.1) that will fly on the International Space station (also known as AMS-02) is composed of:

- a superconducting magnet cooled with superfluid helium having a maximum magnetic field, inside the coils, of 0.7 T where a silicon tracking detector is located, a silicon tracking detector having 8 planes of double-face silicon detectors having 10 µm spatial resolution on the bending direction of the charged particle track and 30 µm resolution in the non-bending direction, a transition radiation detector (TRD) for the electron/hadron separation, a time of flight (TOF) system that will give the general trigger to the experiment, a ring imaging Cherenkov detector (RICH) that will make elemental and isotopic discrimination of cosmic ray nuclei and electromagnetic calorimeter for hadron/electron separation.

The entire apparatus should weight 6700 kg and consume less than 2.3 kW power.

II. THE AMS TRACKER DETECTOR

The tracking system of the AMS-02 instrument is built from silicon detectors. Each elemental detector is a double-side silicon detector having dimensions 40 x 70 mm and 300 µm thickness. It has 640 strips on the p-side and 180 strips on the n-side the two sets of strips are placed orthogonally.
detectors are assembled into ladders each ladder is composed of one row of detectors bonded on the long side with a bonding for each strip on the p-side.

On the n-side the strips in the detectors are connected through a Upilex cable that also carries the bias. The n-side of a ladder is also called K-side while the p-side is also called S-side.

Under the Upilex cable a foam supports the ladders. Depending from the placement inside the magnet ladder can be formed by 7 to 15 detectors.

The detectors are bonded to two PCBs: one PCB hosts the front-end readout circuits for the n-side is called TFEK (Tracker Front End K-side) and the other hosts the front-end readout circuits for the p-side called TFES (Tracker Front End S-side). These PCBs contains VA64_HDR9 readout chips from IDEAS. Every front-end chip has 64 readout channels 16 chips in each ladder; 10 on the TFES and 6 on the TFEK. The PCBs that host the front-end chips also hosts the thermal sensors, the drivers for the analog signal towards the readout electronics, a chip that handles digital commands to the front-end chips (HCC hybrid circuit controller) and decoupling capacitor chips.

The entire tracker has 192 ladders distributed into 8 planes, 6 inside the magnetic field one on the top and one on the bottom for a total of about 200000 channels.

The ladders are connected through cables to the readout cards named TDR (Tracker Data Reduction). Since the decoupling capacitor cannot withstand the bias potential (that varies from 60 to 80 Volts) the digitalization circuit for the n-side are grounded to a potential close to the bias. The decoupling takes place after the ADC and it is done using inductive decouplers.

The power supply and readout electronics is distributed into 8 subunits, each subunit includes a crate and a tracker power distributor (TPD). Each subunit is capable of independent readout and power distribution for 24 ladders.

III. THE POWER SUPPLY SYSTEM ARCHITECTURE

A. The crate and the TPD

The AMS-02 power supply system is interfaced with the main ISS power bus through the unit named PDS (power distribution system). The PDS transform the power from the main ISS power bus at 124 VDC into a secondary 28VDC power and distribute it to the various AMS-02 detectors.

The power supply and readout electronics for each detector is divided into independent subunits (crates and power distribution boxes). As previously stated the electronics for the tracker detector is divided into 8 subunits. A tracker subunit is composed of:

1. A crate (TEC Tracker Electronic crate) hosting 12 readout and data reduction board (TDR), 4 linear post-regulator boards for the power distribution to the front-end circuits (TPSFE tracker power supply front-end) 2 post regulator cards for the distribution of the bias (TBS tracker bias supply) and the higher level data reduction and slow control interface (JINF)

2. A power conversion and distribution unit (TPD tracker power distributor) that includes DC-DC converters for the generation of the different voltages needed to operate the tracker detector system, a slow control interface, and an input filter.

The motivation for this architecture is that different voltage values and different power qualities are needed for the tracker detector. In particular:

- A bias voltage of 80V (or 60V depending on the detector resistivity) is needed to bias the detectors this power should be very low noise and very stable.
- A low, bipolar (± 2V) voltage is needed for the power supply of the front-end electronics also this power should be quite stable a with low noise.
- A third voltage level (3.3V) is needed for the digital electronics, this has less demanding requirements in terms of noise immunity and stability of the previous mentioned voltages.

Because of the various levels of stability and acceptable noise required the bias for the detectors and the power for the front end circuit are generated from DC-DC converter carefully filtered and stabilized by means of linear regulator while the power for the digital electronics comes directly from DC-DC converters.

Another important constraint for the power supply system design comes from the fact that the front-end electronics for the detector side connected to bias should be grounded at bias level because the decoupling capacitor cannot withstand the bias voltage. The minimization of the potential problems arising from short circuit at bias level has lead the designers to the introduction of the power group concept. According to this concept the bias voltage for a crate (24 ladders) is generated by 4 independent linear regulators, this has the consequence that the converter that generates power for the front-end electronics should be sized to power 6 half-ladders ( or ladder sides), in case of short circuit of the bias in one of the ladders 6 ladders lose their bias (6 ladders form one power group) . The size of a power group is a reasonable compromise between size efficiency of the DC-DC converter generating the voltage for the front-end electronics and minimal loss in case of bias short circuit.

Additional constraint is that this electronics should operate in the stray magnetic field of the AMS-02 magnet (maximum 500 G ).

According to those concept the system has been designed and a block scheme is reported in fig.2.
The DC-DC converters included in the TPD are shown on the left side of the backplane while on the right side of the backplane the cards inside the TEC are displayed. The area enclosed in the polygonal is repeated twice in a crate and TPD.

B. The DC-DC converters the S9011B filter and the S9011A TPD controller.

The TPD contains various DC-DC converters, the input filter and the TPD controller.

There are three different kind of DC-DC converter in the TPD, all take input from the 28 V coming from the PDS through the S9011B TPD filter; these converters are:

- The S9051 providing ±2.5 V for the front-end bias and +5.6 V for the ADC inside the TDR. Each module displayed is dual and non redundant. There are a total of 4 dual module 2 for the S-side and 2 for the K-side one single unit of converter for each power group. Each output has 15 mVpp ripple (below 20 MHz) and cross regulation better then 5%. The maximum efficiency is around 78%

- The S9055 providing +120 V for the bias and ±6 V for the linear regulator and current measuring system inside the TBS. There are a total of 2 dual S9055 each power half a crate (one TBS) and it is cold redundant. The output ripple is 20 mVpp on all output (below 20 MHz) and the cross regulation is below 1% for the bias output and less then 10% for the ±6 V outputs.

- The S9053 providing 3.4 V for the digital electronics. There are a total of 2 dual S9053 each power half a crate (6 TDR) and half JINF and it is cold redundant. The output ripple is 20 mVpp on all output (below 20 MHz) and the load regulation is below 4%. The maximum efficiency is around 79%.

The block diagram for one these converters (The S9053) is shown in fig. 3. All converters are forward type converters except for the S9055 which is flyback.

The S9011B Tracker Power Distributor Filter is the input filter of each crate, it is fed with one +28 V DC power supply by the PDS (Power Distribution Box); it includes two stages for the distribution and filtering for the two +28 V power supply branches inside the TPD. Besides the filters, the S9011B includes the circuitry to limit the input capacitors in-rush current at power on. The S9011A Tracker Power Distributor Controller controls the operation and the status of DC-DC converters, according to the block diagram reported in fig. 4. The TPD controller receives two 3.3 V ± 2% power supplies. These are two completely independent branches, one for each Actel FPGA. A 2.5 V power supply for the FPGA core is obtained from the 3.3 V. The protection is provided by a dedicated SSF (Solid State Fuse). In case of short circuit a hiccup logic turns on and then off the SSF with a very small duty cycle. The control logic is embedded inside a HOT and a COLD FPGA, which are two Actel mod. A54SX32A contained in a TQFP144. The two FPGAs monitor the DC-DC converter status and control an input switch in the converters. In order to turn off the DC-DC converters it is necessary to provide at least a 3 mA current to the DC-DC optoisolators.

The S9011A TPD controller board communicates with the slow control logic via a MHV100 LeCroy protocol using LVDS physical layer.
C. TPSFE and TBS.

The Tracker power supply front end (TPSFE) and the Tracker Bias Supply (TBS) are two VME-like boards hosted in the crate that also contains readout, data reduction and slow control interface board. These boards have VME standard mechanics but different pin assignment in the connectors J1 and J2.

The TPSFE is a 12 channel linear regulator. Each channel provides a +2.1 V and a –2.1 V volts outputs; the channels are arranged into two six-channel groups, named K-Side and S-Side respectively. The K-side linear regulator will be kept at the bias voltage of the silicon ladders (60V-80V) from now on called Vbias, the S-side will be kept at ground level (0V) from now on called Ground. Each group features a common floating return (gnd K and gnd S). The linear regulars also have burp mode current protection. The status of each regulator can be monitored via slow control.

Moreover the board features:
- 6 LVTTL outputs for the TDR boards turning off
- 6 inputs for monitoring the TDR boards
- 1 LVDS link for communicating with the JINF
- 2 links for monitoring the temperature via DS1820 sensors.

The first two features mentioned above are because the TPSFE card also acts as a slow control interface for the TDR, through the TPSFE is possible to switch off or restart a TDR board. A block diagram for this board is shown in fig. 5.

![Fig.5 Block diagram for the TPSFE](image)

The TBS is the board which manages the regulation, control and monitoring of the bias voltages of the silicon detectors: the board regulates and distributes the bias for the detectors. Each board supplies 2 Power Groups (PG). The TBS thus provides:
- 2 “HOT” bias linear regulation channels, which can be set on two different levels (60 V and 80 V) via slow control, for the linear regulation and protection of the silicon bias voltages;
- 2 “COLD” bias linear regulation channels, which can be set on two different levels (60 V and 80 V) via slow control, for the linear regulation and protection of the silicon bias voltages;
- 12 channels for –2 V silicon bias return with current monitor.

Moreover the board includes:
- ADCs for the readout of the output power supply voltage and absorbed current of each ladder (such readout is performed on the –2V return).
- Filter for the noise suppression (on the 120 V line) made up by a RC circuit;
- Control electronics (ACTEL FPGA) for monitoring the operation status, the digitized parameters readout and the setting of the TBS controls;
- LVDS link for the interface with the slow control system for the control and/or readout of the Control electronics;
- Electronics for the monitoring and control of the JINF board;
- Electronics for the monitoring of the operating temperature of the board via slow control on dedicated serial lines.

The bias linear regulator receives +120 V ± 10% from the bus and regulates it at 80 V ± 5 %, which can be brought to 60 V ± 5 %, via a control input connected to the FPGA. Moreover the circuit features an OFF/ON input and an output for the voltage monitor.

The regulator is protected by a foldback limitation with a 500 µA maximum current and a 350µA (@80 V) short circuit current.

The regulator ramps up to 80 V in 7 seconds circa (with 30 µF on the output).

The return regulators have two purposes: establishing the operation point of the ladders at –2 V and measuring the absorbed current. As for the TPSFE also for this board the control logic is embedded into a HOT and a COLD FPGA, which are two Actel mod. A54SX32A contained in a TQFP144, and the communication protocol is MHV100 LeCroy protocol through a LVDS physical layer. The block diagram for this board is shown in fig. 6.

![Block diagram for the TBS](image)

IV. THE SPACE QUALIFICATION TESTS

The power supply system development and production is divided in 4 phases

Phase 1 EM (Engeneering Model) development of boards where only functional and integration test have been performed.

Phase 2 QM1 (Qualification Model 1) where vibration, thermovacuum, and EMC/EMI tests are performed on single boards (2 crates and 2 TPD produced).

Phase 3 QM2 (Qualification Model 2) the cards will undergo a full set of vibration, thermal stress and thermovacuum tests, these tests will be done at crate or TPD level (1 crate and 1 TPD produced).

Phase 4 FM and SM (Flight and Spares Models) the entire system will be produced in 10 crates/TPDs (8 flight and 2
spares) and will undergo a reduced set of vibration, thermal stress and thermovacuum tests at crate level.

The first two phases of the production will take place in Europe phase 3 and 4 will be performed in Taiwan at CSIST and NSPO.

Currently we have finished the QM1 production and testing phase so single board level qualification test will be presented here; however the QM2 will be done at the same condition of the QM1 tests but at crate or at TPD level. For the first integration and functional test of the boards inserted in a reduced tracker with the same functional element as the total tracker see ref.[2], however those test gave encouraging results so the design of the boards was modified very little from Phase 1 to Phase 2.

The power supply system of the AMS-02 tracker was designed using COTS components; pre-design radiation tests were performed on all semiconductor components used [3],[4],[5].

On QM1 modules we performed the following tests:
- Thermal vacuum tests.
- Thermal mechanical vibration tests
- EMC/EMI tests.

Thermal Vacuum tests has been performed to verify the operation of the various cards and to detect potential hot spots inside the card itself, for this purpose thermal sensors were placed in thermally critical area of the various cards. The thermo-vacuum tests have been performed into a TY 2000 WC Angelantoni Climatic Chamber, inside the chamber the cards were placed into a aluminum vacuum vessel connected to a two stage (rotary and turbomolecular) pump, the vacuum was monitored by means of a pirani gauge and was below 10^{-2} mbar during most of the test.

The thermal cycles were performed considering the maximum and minimum operating temperature (card under test powered) and the maximum and minimum non-operating temperature (card under test unpowered). A scheme of the thermal cycles is reported in fig.7.

At the end of the cycles and during the test all cards remained functional no hot spots were detected in any card namely the temperature difference between critical points and dissipation layers was always below 10 °C.

The Vibration test shall be intended as thermal-mechanical stress test at card level. It is divided in three phases:
1. First thermal stress test
2. Vibration test
3. Second thermal stress test

Phase 1 and 3 test shall be performed in the same climatic chamber used for the thermo-vacuum test according to the following diagram (fig.8).

where Tmin = -45 °C and Tmax = 85 °C . Phases 1 includes 10 thermal cycles and phase 3 includes 5 cycles the duration of a complete cycle is 2 hours.

Phase 2 shall be performed in a shaker vibrating the card for 4 minutes for each vibration axe according to the random vibration spectrum showed in fig. 9.

During the thermal cycles and vibration test the card is not powered. At the end of each test phase a complete functional test was performed . All cards passed the test because all voltages are within the specification and command and statuses do not show any failure. Furthermore all resonance frequencies of the cards were above the safety limit of 50 Hz.

The EMC/EMI tests were done according to the following specifications:
MIL-STD-461E CE-101
MIL-STD-461E CE-102
MIL-STD-461E CS-101
MIL-STD-461E RE-101
MIL-STD-461E RE-102
MIL-STD-461E RS-101
MIL-STD-461E RS-103

Fig.9 Random vibration spectrum.

The EMC tests have been performed with the Laboratory of Electromagnetic Characterization of Perugia University, Faculty of Engineering, Via Pentima Bassa, 21 – 05100 Terni in the semi-anechoic chamber having the following characteristics:

- Dimensions: 9.15m x 8.00m x 5.55m.
- Automatic Mast for antenna movement.
- Electromagnetic absorbing material: ferrite. characteristics: 30MHz – 1GHz.
- Frequency range for shielding: 10 kHz – 18 GHz.

Both conducted and radiated electromagnetic emissions in all cards were below the limits sets by the MIL-461E standard, the operation of the card remain unperturbed after the susceptibility tests in all cards.

V. CONCLUSIONS

The AMS-02 tracker power supply system was described in this paper, a general overview of the test results was also given. The design and basic architecture of power supply system of the tracker has been used by all other AMS-02 subsystem as a base for their design.

Currently phase QM2 of the production is finished and we are looking forward for the qualification test at crate level. The Flight models and the spare should be produced within year 2005.

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VII. REFERENCES


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