Surface Mount Capacitor Loop Inductance Calculation and Minimization

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Abstract: This paper proposes a simple method to calculate PCB surface mount capacitor loop inductance using magnetic field equations for a small current loop. The equations proposed in this paper are simple enough to be programmed into software packages such as MathCad, Matlab, or even a simple spreadsheet. These equations are also verified against experimental data to show good correlation between the theoretical calculations and the actual measurements. Using these equations, the author further optimizes the capacitor footprint and via placement geometry to reduce the capacitor loop self-inductance for printed circuit board designs.

INTRODUCTION

As the clocks of semiconductor devices get faster and faster, the high frequency noise on the logic common (typically known as "ground bounce" or "delta I noise") has become a more serious EMI problem than ever before. This noise is usually generated by fast switching semiconductor devices with clock frequencies up to 400 MHz drawing more than 10 A of current from the power bus. An ASIC, designed using CMOS technology, consumes little or no current under static conditions. But it draws current to charge and discharge gate and diffusion capacitance while it is changing states, so the current drawn by the ASIC is the transient current corresponding to the rising and falling edges of the clock [1]. Due to finite power bus impedance, this transient current creates a voltage drop in the current path. This switching noise propagates along the power and ground layers of the PCB and affects all devices (including the I/O drivers) on the board. Due to cost, heat dissipation, manufacturability, and ease of design reasons, building an airtight metal box to contain the EMI emission is impractical. Even if an air-tight metal box were a feasible solution, it still would not solve all the EMI problems since any unshielded I/O cable leaving the box can still radiate EMI. The most effective solution is to filter this noise at its source -- the switching ASIC. One can accomplish this by either adding adjacent power and ground layers in the board to increase inter-plane capacitance or adding capacitors to the power bus close to the ASIC to lower the impedance locally. Adding adjacent power and ground layers is very effective in filtering high frequency noise, but it can also be costly if many layers are needed. Adding capacitors to the board is a relatively low cost solution, but the inductance of vias and other mounting structures (as shown in figure 1) can increase the capacitor impedance at high frequency (figure 2). Due to this inductance, a capacitor with a randomly chosen value most likely will have little or no effect on this switching noise. The purpose of this paper is to determine the total self-inductance of the current path of a surface mount multi-layer ceramic capacitor tied to power and ground planes using one via on each terminal through theoretical calculations and experimental results.

There have been many papers previously published that deal with inductance calculations [2-6]. Some of them also provide equations for calculating capacitor lead inductance. But these papers mostly derive the equations using partial inductance analysis, which may be complex for surface mount component applications. In this paper, the author uses the magnetic field equation for a small loop to calculate the self-inductance for the loop. By knowing this inductance, one can calculate the resonance frequency of the capacitor geometry so that an appropriate capacitor value can be used to lower the power bus impedance for a certain frequency range (figure 2) (e.g., the clock frequency or its harmonics).
ASSUMPTIONS

The following assumptions are made in deriving the magnetic field equations for the loop inductance calculations:

1. The current loop is short compared to a quarter wavelength of the frequency under consideration, so that the static field solution can be used.

2. The current is uniformly distributed on the surface of the conductors (i.e., vias and ground planes), since the diameters of these vias are small and their materials are assumed to be perfect conductors.

3. For simplicity reasons, the capacitor is modeled as a cylindrical wire made of perfect conducting material. This assumption is made because the loop inductance is mainly determined by the loop geometry, so replacing the capacitor by a wire should not change the loop inductance significantly.

4. The DC planes on this printed circuit board are physically large compared to the diameter of the vias and capacitor, so due to current spreading effect, the magnetic field generated by the current on the DC planes is insignificant compared to the field generated by the current on the vias and capacitor.

CALCULATION

Vector Poisson's equation [7]:

\[ \nabla^2 A = -\mu_0 J \]  \hspace{1cm} (1)

Apply this equation to a thin wire in cylindrical coordinates and solve for \( A \) at a point \( P \) located at a distance \( r \) from the wire [8] (see figure 3):

Figure 1: A surface mount capacitor is placed on a 10-layer board with 2 vias. The current loop consists of 2 vias and the capacitor itself. The loop area is set by the spacing between the vias and board thickness.

Figure 2a: This circuit model is used in the SPICE simulation to calculate the capacitor impedance for a 470 pF capacitor and a 0.047 uF capacitor. See figure 2b below.

Figure 2b: The capacitor model is driven with a 1 A current source, so the voltage developed across the capacitor is equal to the capacitor impedance. The impedances for a 470 pF capacitor and a 0.047 uF capacitor are shown in this plot. The 470 pF capacitor has lower impedance in the 100 MHz - 300 MHz range, but the 0.047 uF capacitor has lower impedance below 100 MHz.
Due to cylindrical symmetry, we have

\[ \frac{\partial A_z}{\partial \phi} = 0, \]

so

\[ B = -a_0 \frac{\frac{\partial \mu J}{\partial r}}{4\pi} \left[ \frac{1}{(L_1^2 + r^2)^{0.5}} + L_1 \right. \]

\[ \ln \left( \frac{(L_2^2 + r^2)^{0.5} + L_1}{(L_2^2 + r^2)^{0.5} - L_2} \right) \]

\[ = -a_0 \frac{\frac{\mu I r}{4\pi}}{(L_1^2 + r^2)^{0.5}} \left[ \frac{1}{(L_1^2 + r^2)^{0.5} + L_1} \right. \]

\[ \left. - \frac{1}{(L_2^2 + r^2)^{0.5} - L_2} \right]. \]

The above equation calculates the magnetic flux density generated by the current on a wire for a point (in space) specified by \( L_1, I_z, \) and \( r. \) The capacitor current loop in figure 1 can be modeled as 3 straight wires interconnected together with 2 conductive planes. One can assume that due to current spreading effect, the magnetic field (or flux) generated by the current on the conductive plane is insignificant compared to the magnetic field generated by the 3 wires, as shown below [9]:

\[ \nabla \times \mathbf{H} = \mathbf{J}. \]

If the current density \( \mathbf{J} \) is low, \( \mathbf{H} \) will be small and \( \mathbf{B} \) will also be small. Therefore, the magnetic flux, \( \mathbf{B}, \) inside this current loop is simply the superposition of the flux generated by the 3 wires. The total flux inside this loop is calculated by the following expression [10]:

\[ \Phi = \int \mathbf{B} \cdot d\mathbf{s}, \]

where \( S_1 \) is the surface bounded by the current loop. The self-inductance of a small current loop can be calculated as follows [11]:

\[ L_{\text{self}} = \frac{\Phi}{I}, \]

where \( I \) is the loop current which generates the flux \( \Phi. \)

![Figure 3: A straight wire of length \( L_2 = L_1 + L_3 \) carries a current \( I \).](image)

A meshed surface plot of the magnetic flux density \( \mathbf{B} \) for the current loop in figure 1 is shown in figure 4. A simple observation is that the flux density does drop off by the \( 1/r \) relation as \( r \) increases, so this result is as expected. The inductance for a current loop in a printed circuit board with the vias spaced 0.32 inch apart as shown in figure 5 is calculated to be 3.5 nH. This is a somewhat typical via placement for a 1206 capacitor. An inductance table is generated below for different via length and via spacing.
D = via length (inch)
W = via spacing (inch)

<table>
<thead>
<tr>
<th>W</th>
<th>1.2</th>
<th>1.5</th>
<th>1.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>.17</td>
<td>1.6</td>
<td>1.9</td>
<td>2.2</td>
</tr>
<tr>
<td>.22</td>
<td>1.9</td>
<td>2.3</td>
<td>2.7</td>
</tr>
<tr>
<td>.27</td>
<td>2.3</td>
<td>2.7</td>
<td>3.5</td>
</tr>
</tbody>
</table>

This table shows how the loop self-inductance is affected by different via lengths and spacings. On a printed circuit board, the via length can be shortened by moving the power and ground planes closer to the surface of the board where the surface mount capacitors are placed. The via spacing can be reduced by placing the vias on the inside of the capacitor soldering pads, as shown in figure 6.

Equation (5) does have its limitations. Intuitively, one can guess that as the loop size is further reduced and the DC planes are moved closer to the SMT capacitor, the flux density in the loop will increase and the current density on the DC planes will become significant. Also, for the case shown in figure 7, in which the capacitor is placed next to the DC planes, so that the majority portion of the current loop is no longer closed, the equation may not provide accurate results.

Figure 5: The mounting pads and connecting vias for a 1206 capacitor are shown. With via lengths equal to 0.050 inch, the resulting loop self-inductance for this geometry is approximately 3.5 nH.

Figure 4: This is the meshed surface plot of the magnetic flux density for the current loop shown in figure 1. The flux density drops off by the 1/r relation as r increases.

Figure 6: These are the same mounting pads as that of figure 5 but with the vias placed on the inside of the pads.

Figure 7: This is a 10 layer board with the power and ground layers placed next to the surface mount capacitor. Equation (5) will not provide accurate results for this configuration due to the open portion of this loop.
**EXPERIMENTS**

The inductance for different loop sizes is measured. The measuring method is given below:

1. Solder a wire (30 AWG) to a two-layer pcb (9" x 3") as shown in figure 8a.

2. Use a scalar network analyzer to perform a frequency sweep on one end of the pcb. Measure the transmitted signal at a point near the wire loop on the parallel planes of this pcb as shown in figure 8a, top view. This setup measures the transfer impedance ($S_{21}$) of the circuit across a frequency range.

The equivalent circuit (lumped model) for this setup is shown in figure 8b. This circuit has a natural resonance frequency (figure 8c). From this resonance frequency, one can calculate the inductance $L$ of this circuit if the capacitance $C$ is known. $C$ is equal to 0.4434 nF, and it is determined from the pcb dimension and its dielectric constant ($\varepsilon_r = 4.6$). The table below shows the measured and calculated inductance for different loop dimensions:

<table>
<thead>
<tr>
<th>$W \times D$</th>
<th>measured</th>
<th>calculated</th>
</tr>
</thead>
<tbody>
<tr>
<td>.340 x .263</td>
<td>10.6</td>
<td>11.0</td>
</tr>
<tr>
<td>.210 x .223</td>
<td>7.1</td>
<td>7.2</td>
</tr>
<tr>
<td>.210 x .173</td>
<td>5.9</td>
<td>5.7</td>
</tr>
<tr>
<td>.140 x .163</td>
<td>4.3</td>
<td>4.2</td>
</tr>
</tbody>
</table>

The error in the calculated inductance in table B is reasonable — less than or equal to 3.8%. This is expected due to the assumptions made in the derivation of the equations. Also, the integral for the magnetic flux (equation 7) inside the current loop is calculated numerically by dividing the loop area into 2500 small squares and computing the flux density for each square. The results would be more accurate if more squares were used for this integral calculation.

The plot in figure 8c has more than one resonance. This is because at high frequency, this two-layer pcb becomes a parallel-plate waveguide with no terminations, so the lumped circuit model in figure 8b is no longer applicable. This waveguide has a natural resonance frequency due to the standing wave built-up between the two plates. This resonance frequency is 635.2 MHz, which has a wavelength of 8.8 inches inside the pcb dielectric, and the pcb length is 9 inches. The wavelength of the resonance frequency closely matches the dimension of the board. The transfer impedance frequency response of the pcb without the wire loop is plotted in figure 8d, and the resonance frequency (635.2 MHz) in 8d does match the resonance frequency in 8c.

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**Figure 8a:** This is the top and side view of a two-layer pcb with a small wire loop connecting the top layer to the bottom layer at the center of the board.

**Figure 8b:** This is the lumped circuit model for the pcb in figure 8a. This model is used for the loop self-inductance calculation.
current loops. They are useful for determining the resonance frequencies of surface mount capacitors. The experiments performed in this paper also show that to reduce the capacitor current loop self-inductance, the vias on the capacitor terminals must be placed as close together as possible, and the DC planes must be placed close to the surface of the board. By doing this, the loop size is reduced and the loop self-inductance is also reduced. Experiments have shown that it is possible to reduce the capacitor current loop self-inductance for a 0805 foot-print capacitor down to 0.3 nH or less.

**ACKNOWLEDGMENT**

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**REFERENCES**


