Grounding Optimization Techniques for Controlling Radiation and Crosstalk in Mixed Signal PCBs

DHEENA MOONGILAN
Bell Laboratories
Innovations for Lucent Technologies Inc.
Holmdel, NJ 07733

Abstract: Analog, digital and RF signals are being widely used on single Printed Circuit Boards (PCBs) for network communication, multimedia, and wireless signal processing applications. Separate ground islands or segments are provided for analog, digital, and RF circuits to minimize ground noise coupling from high speed digital to sensitive analog or RF circuits. The noise level for digital cellular equipment should be as low as 0.3 μV. Isolated or improperly interconnected ground islands often become high-frequency resonant circuits or patch antennas. This paper describes techniques or procedures for determining optimized grounding for high-frequency mixed signal single board PCBs for minimizing crosstalk and radiated emissions.

I. Introduction:

Most digital to analog converter (DAC) and analog to digital converter (ADC) data sheets specify spurious signals over the full Nyquist range [1] extending from DC to one half of the data sampling rate. The high-frequency harmonic and non-harmonic components are seldom specified on the assumption that they can be eliminated using conventional EMC techniques such as filtering, grounding and isolating. The high-frequency radiation and interference problems due to ground resonance are often discovered during the system EMC and crosstalk measurement. The ground resonance issues must be addressed at early design stages, otherwise, expensive and time-consuming design iterations are necessary to solve this problem. Due to complexity of circuit parameters and geometry of PCB, accurate simulation models are not currently available. This paper describes two practical inexpensive and less time consuming grounding optimization techniques to control the ground resonance and related radiation, crosstalk and signal jitter.

II. Grounding techniques for Mixed signals:

Single PCB: Several recent publications suggest grounding philosophies for single board high speed ADC and DAC converters [2,3]. Most popular is a recommendation to use split planes for power, and ground with single point interconnection between the split ground planes as shown in Figure 1. The single board technique is preferred because in a multiple PCB card system signal interconnection to digital, analog or RF boards must be routed through the mother board or backplane using longer traces and inductive connector pins. Longer traces entail larger loop areas and an increase in radiated emissions.

Split Planes: In single board PCB, a common ground layer for analog, RF, and digital cannot be used because the noise immunity level for certain RF and analog circuits is as low as 0.3μV. A common power layer cannot be implemented because of noise immunity problems and different voltage requirements. Further, a complete overlapping of separate power and ground layers for analog, digital, and RF cannot be used to minimize capacitive coupling of noise between adjacent layers. Therefore, it is customary to use split ground and power planes or islands for analog, RF, and digital circuits.

Ground interconnection: In order to provide short return current paths for interconnecting mixed signal traces, the different ground islands cannot be isolated. The interconnection of grounds is also necessary to allow controlled impedance microstrip or strip transmission lines between mixed signal chips. The return current of unbalanced high-frequency signals tightly flows as a mirror image of the trace on adjacent power or ground layers [4]. If ground interconnection is not provided, the return current will flow through a longer path creating a larger loop area.

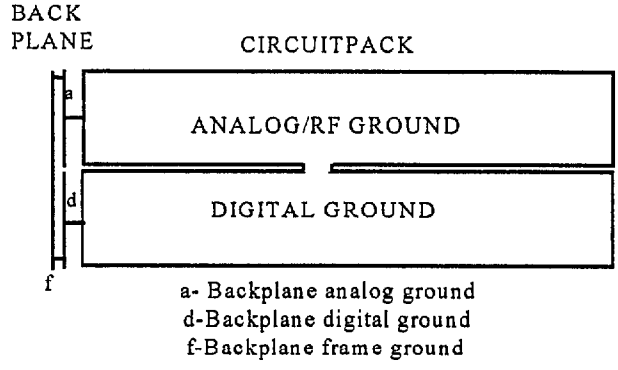

Figure 1. Single point interconnection in a mixed signal split ground plane.

Noise drain path: Common-mode noise in circuit boards is generated due to inductive, and capacitive coupling noise from adjacent traces and noisy components. Applying conventional EMC rules noise coupling can be reduced. The decoupling capacitors between power and ground traces reduce loop area by short-circuiting the differential noise voltages. The current generated by short-circuits is circulated as common mode current on the power and ground layers on different mixed signal islands. The common-mode noise should be drained to frame ground to avoid daisy-chaining through different signal grounds. The placement of components and ground islands should be such that noise current generated on grounds shall be directly drained on cardcage/chassis through their respective backplane grounds and then to the

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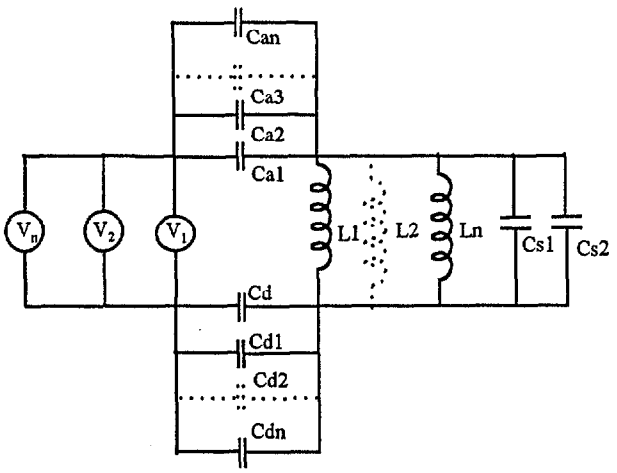
backplane frame ground plane layer as shown in Figure 1 of Reference [5]. If a cardcage or backplane does not exist, noise shall be drained directly into a large chassis ground or drain plate as shown in Figure 4.

III. Ground interconnection noise and problems:

Single point ground interconnection technique in mixed signal single PCBs is normally useful for controlling radiation at low frequencies (< 10 MHz) circuits. In high-frequency large PCBs with multiple interconnecting traces between mixed signal islands, single point ground interconnection is not practical. These grounds are unintentionally interconnected through stray capacitance in common ICs, backplanes, filters, split plane gaps, PCB connector pins, vias on other layers, and other unknown inductive paths. It is necessary to reduce loop area, high inductance paths, and loop resonance to reduce radiated emissions. For PCBs that use single point interconnection (see Figure 1), the signal leads sometimes must be routed through long inductive paths if chips in analog and digital sides are not placed nearby. To reduce large inductive paths, additional interconnection between grounds must be provided, but several interconnections emulate a single ground layer and increase the crosstalk. Therefore, interconnections should be narrow and shorter and the number of interconnections should be as few as possible. Both single and multipoint interconnections often produce ground resonance due to unintentional high frequency current loops due to improper or unintentional interconnections as explained earlier in this section. If the ground resonance frequency happened to be one of the circuit operational frequencies, its harmonic or spurious component, radiated emissions on the resonance frequency may increase by 5 to 15 dB as compared to non-resonance frequencies.



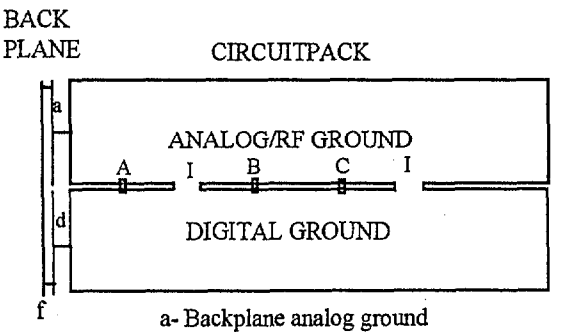
Ca - capacitors on analog side
Cd - capacitors on digital side
Cs - stray capacitors between gap
L1,L2 - interconnection signal trace ground impedance
V1,Vn - signal voltage or ground bounce

Figure 2. Some identified circuit components in split ground plane.

Most currently available mathematical and computer simulations are not able to accurately predict unintentional current loop resonance due to the following complexities: (a) in addition to board power to ground layer capacitance, trace to power capacitance, trace to ground capacitance, the chip capacitance and on-board decoupling capacitors and their effective distribution must be known;
(b) the current flow distribution on ground and power layers must be known;
(c) the effective inductance path between circuitpack, backplane and connector pins cannot be determined accurately;
(d) too narrow interconnecting paths develop potential difference between grounds and wider paths entail more noise current coupling;
(e) the primary contributor to resonance is interconnection ground path inductance and ground gap capacitance. The ground and power layer capacitance and inductance do not normally form a resonance circuit themselves due to reduction in Q-factor by chip and circuit resistors. However, power and ground capacitance may contribute to the gap loop resonance in parallel or series combination. The effective gap capacitance has several variables: the length, width, dielectric between ground gap, dielectric above and below the gap. The interconnection ground path inductance is easily determinable, while effective capacitance is difficult to determine. The complexity of the equivalent circuit is shown in Figure 2;
(f) The gap loop resonance is dynamic and changes with circuit electrical mode of operation;
(g) prototyping and "trying out" experimental model boards is expensive and requires longer design times.

IV. Ground optimization techniques:

Two practical ground optimizing solutions are described in this paper. First method uses backplane frame ground as the noise drain path and the second method uses a drain plate attached parallel to the circuit boards. The second method can be used in backplane based systems or non-backplane based systems such as mother board. Both methods use additional ground interconnections to modify the loop resonance. The effective interconnections that contribute low crosstalk, jitter, and radiation is determined by test. Ground optimizing steps are indicated below:



a- Backplane analog ground
d-Backplane digital ground
f-Backplane frame ground
I-Ground interconnection for inter signal routing
A,B,C - Zero Ohm resistors for optimizing radiated emissions.

Figure 3. Ground interconnection for optimizing radiated emissions - Method 1.

First method - Backplane noise drain path:
(1) determine real estate necessary to carry trace return current (normally 3 times the trace width [6]);

(2) provide minimal 'n' number of interconnections, so that inter mix-mode signals are routed between split ground islands through reasonably shorter paths;
(3) provide additional '2n' interconnections approximately equal distance. These interconnections should be through low inductance zero ohm resistors;
(4) analyze circuit operation for crosstalk and optimize the number of interconnections by eliminating 'n' number or reducing the number of zero ohm resistors that may contribute to crosstalk;
(5) perform radiated emission tests and optimize ground interconnection for several zero ohm resistor combinations, so that circuit resonance does not fall on the clock harmonic, or any spurious component and overall radiated emissions are below the specification limits;
(6) repeat steps 4 and 5 if necessary.

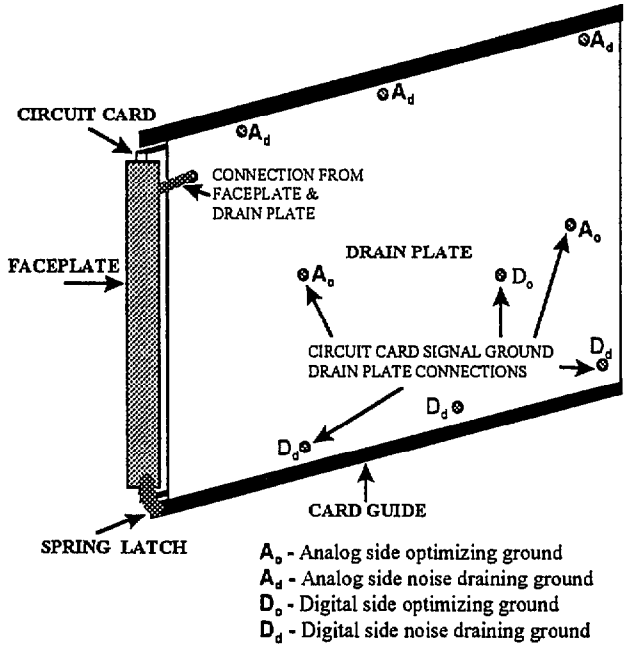


Figure 4. Ground interconnection for optimizing radiated emissions - Method 2.

Second Method - Circuitpack with noise drain plate:
(1) use steps 1 and 2 of first method;
(2) provide '2n' solder mask removed plated-through holes for ground layers approximately equal distance on either side of mixed mode signal islands. Interconnect the plated through holes to drain plate through low inductance screws;
(3) analyze circuit operation for crosstalk and optimize the number of interconnections by eliminating 'n' number or reducing the number of interconnections that may contribute to crosstalk;
(4) perform radiated emission tests and optimize interconnections for several combinations, so that circuit resonance does not fall on the clock harmonic, or any spurious component and overall radiated emissions are below the specification limits;
(5) repeat steps 3 and 4 if necessary.

V. Experimental Results:

The author has implemented both methods on several systems. In the first method, although interconnections through capacitors can be made, this does not often yield good results because of self resonance frequency of the capacitors, difficulty in predetermining the value of capacitor, non-standard capacitor values are required, and large change in resonance frequencies, thus shifting the problem from low end to high end of the spectrum. In the second method, ground resonance is less severe than the first method. Normally, an interconnection at every 3" to 4" is sufficient. Interconnections to the drain plate at the middle of the board help to solve resonance problems. Interconnections at the edges of the board are normally used as noise current drain paths similar to frame ground connections to backplane in the first method. In most products, an average reduction of 5 to 15 dB radiation level was observed while implementing the first method, compared to a reduction of 3 to 5 dB in the second method.

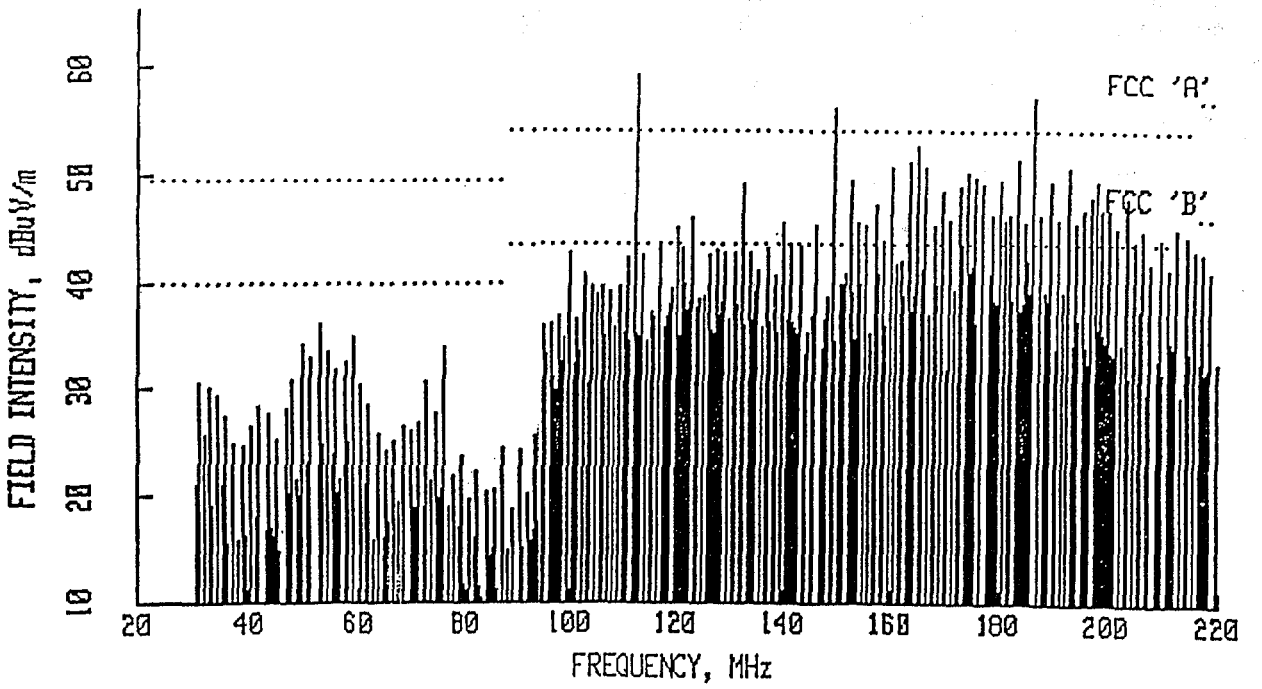
An example of optimized radiated emissions using the first method is shown in Plots 1 through 6. The test circuitpack had analog, RF, and high speed digital ICs. The circuit board is a 10 layer 14.3" long and 8.5" wide card. There were two ground interconnections for signal routing spaced approximately 6" apart. A total of 6 zero ohm resistors were used as additional ground interconnections and reduced to 3 for radiated emission optimization. For this test board, all three additional ground interconnections were required for lower radiated emissions as shown in Plot No.2. The radiated emissions tests were performed in a 3 m absorber-lined shielded room.

VI. Conclusions:

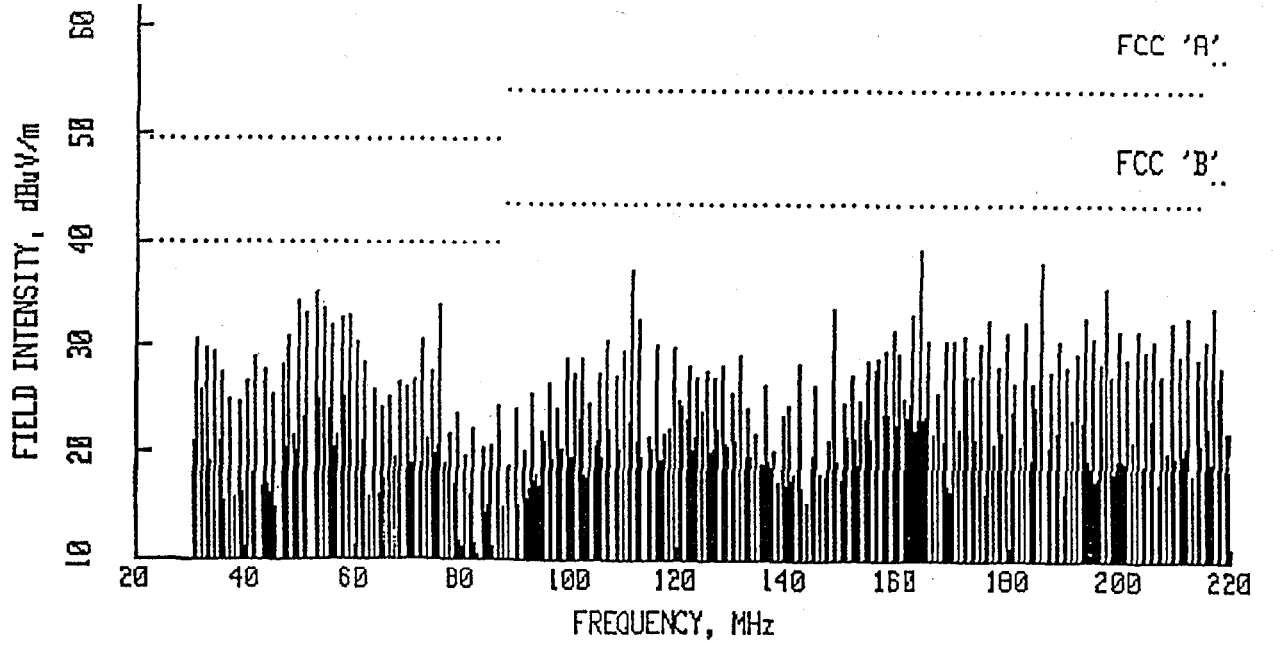
In mixed-signal single PCBs, the radiation, crosstalk levels and intrinsic signal jitters change with ground interconnection points and the number of additional ground connections. Both methods are found to be more economical and take less time for solving radiation, crosstalk and jitter problems in a mixed signal environment. In the second method, the last layer of the circuit board can be used as drain plate. This is not as efficient as drain plate because pads, components, plated-through holes radiate themselves and reduces the availability of real estate. Both methods do not change the system architecture or use extra expensive hardware for optimizing the ground. These methods use some additional ground interconnections or disconnection on existing grounding architecture to reduce crosstalk, jitter and improve radiated emission margins.

VII. References:

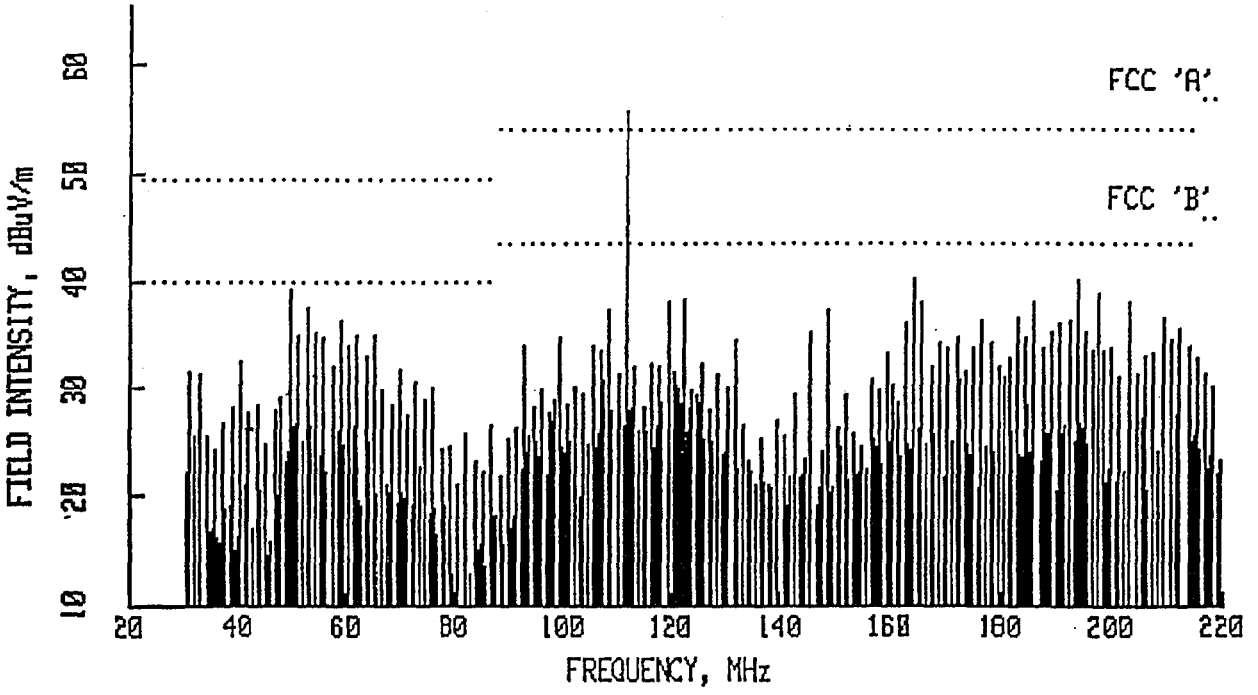
[1] H. Nyquist, "Certain topics in telegraphic transmission theory," Trans. AIEE, Vol.47, pp 617-644, April 1928.
[2] W. Kester, "A grounding philosophy for mixed-signal systems", Electronic Design, Special analog issue, June 23, 199, pp 29-38.
[3] W. Kester and J.Bryant, "Grounding in high speed systems", High speed Design techniques, Analog Devices, 1996, Chapter 7, pp 7-27.
[4] D. Moongilan, "Skin effect modeling of image plane techniques for radiated emissions from PCB traces", IEEE 1997 International symposium on EMC, pp308-313.
[5] D. Moongilan, "Skin effect modeling of radiated emissions from backplanes", IEEE 1996 International symposium on EMC, pp332-337.
[6] R. Faraji-Dana and Y.L. Chow " The current distribution and ac resistance of microstrip structure", IEEE trans Microwave Theory and Tech. Vol. MTT-38, No. 9, pp1268-1277, September 1990.



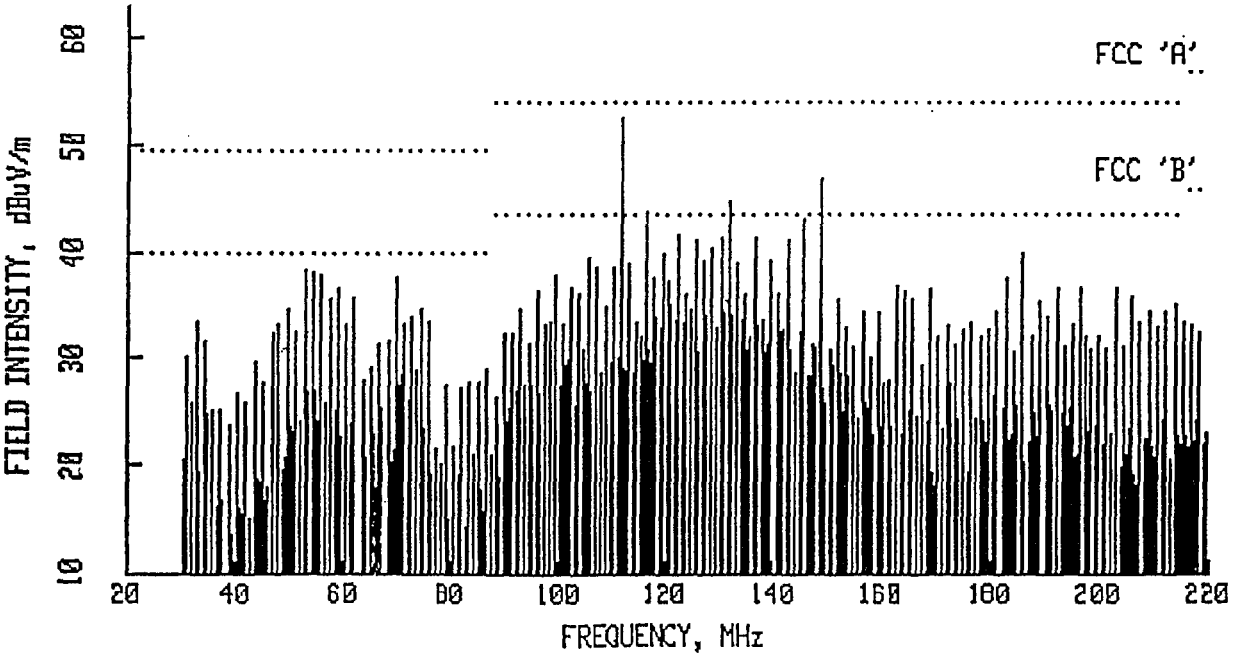
Plot 1. No additional zero ohm ground paths.



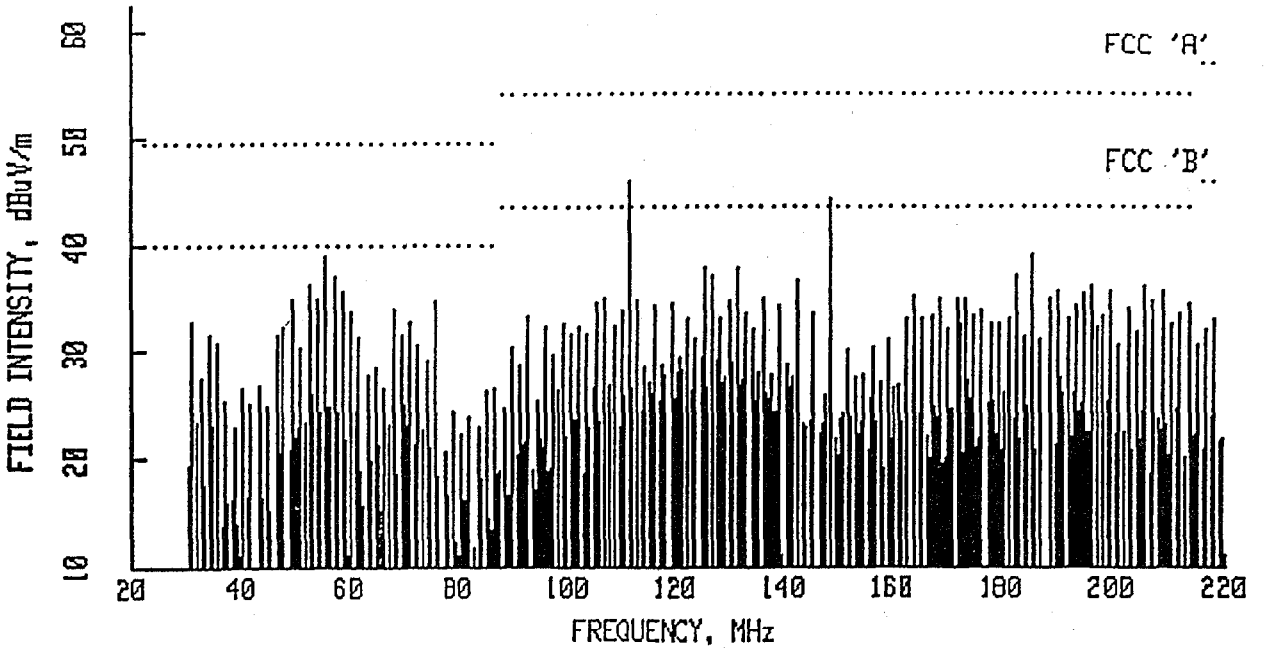
Plot 2. Three additional zero ohm ground paths.



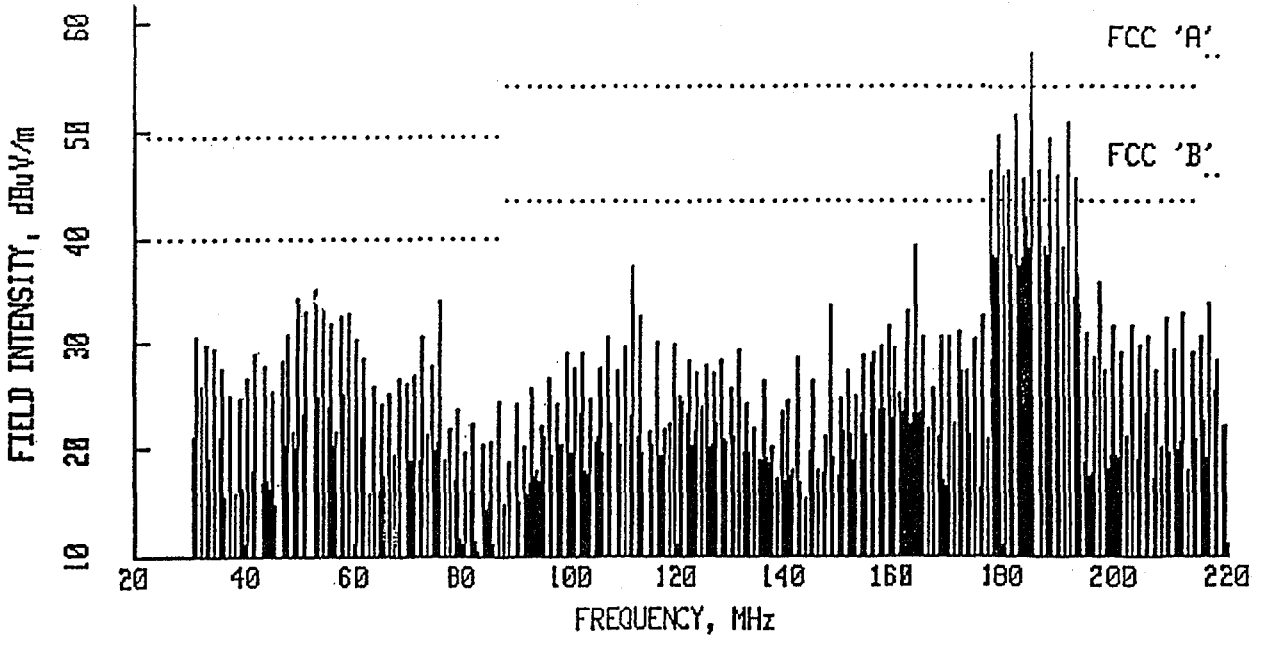
Plot 3. Additional zero ground paths 'A' and 'B' connected.



Plot 4. Additional zero ground paths 'B' and 'C' connected.



Plot 5. Additional zero ground paths 'C' and 'A' connected.



Plot 6. Additional zero ground path 'C' connected.