Simulated and Measured I-V Characteristics of FD SOI-NMOS Transistors Modified by the Self-Heating Effect

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Abstract

Short-channel (1.0 and 2.0 \(\mu\)m) fully-depleted SOI NMOSFET’s were submitted to moderate bias voltages and exhibited the known negative differential output conductance effect. MEDICI simulation of device electrical behavior employing two-dimensional analysis has been used, including lattice heating, impact ionization and total energy balance models. Device structure was simulated by SUPREM IV according to processing parameters used on manufacturing the experimental samples. Simulated and experimental \(I_{DS} \times V_{DS}\) curves show a remarkably good agreement. Theoretical \(I_{DS} \times V_{DS}\) curves, without lattice heating, were also simulated and agree with preliminary experimental results obtained in a self-heating free narrow pulse test, which indicates an \(I_{DS}\) about 30% higher than that for DC curves when \(V_{GS} = V_{DS} = 6V\) in both cases.

1. INTRODUCTION

Employing Silicon-On-Insulator (SOI) materials in the fabrication of modern IC has been proposed as an alternative to improve circuit electrical performance, in addition to simplify their fabrication process [1], which generally results in better yields. Most advantages come from the buried oxide layer, typical in those materials, which makes device isolation easily obtainable, reduces parasitic capacitance and \(pn\) junction collecting volumes and allows for the fabrication of fully-depleted devices. Additional advantages such as latch-up free, denser and faster circuits, radiation hardness, better performance at high temperatures, reduced power consumption, and steeper sub-threshold behavior are also ensured.

However, this buried oxide acts as a heat transfer barrier due to its much lower thermal conductivity as compared to that of silicon. Consequently, the buried SiO\(_2\) causes self-heating during normal device operation [2-5]. For a correct modeling, this effect must be included in electrical simulation. Using MEDICI [6] simulator, this can be accomplished by solving lattice heat, total balance energy, Poisson’s and continuity equations. Carrier mobility degradation is the most important effect due to self-heating. Under high power dissipation, mobility degradation effect is dominant over the typical Early effect, and a negative channel differential output conductance is observed [7].

2. EXPERIMENTAL

Fully-depleted SOI NMOS transistors with 1.0, 1.5, 2.0 and 3.0 \(\mu\)m length and 50 \(\mu\)m wide nominal channel mask dimensions were used for experimental measurements. Primary device and process characteristics of the experimental samples are the following:

- Front oxide thickness, \(t_{oxF} = 30\) nm
- Back oxide thickness, \(t_{oxB} = 400\) nm
- Si transistor layer thickness, \(t_{Si} = 85\) nm
- Channel doping concentration, \(N_A = 6 \times 10^{16}\) cm\(^{-3}\)
- Substrate concentration, \(N_B = 1 \times 10^{15}\) cm\(^{-3}\)
- Source and Drain concentration, \(N_D = 1 \times 10^{19}\) cm\(^{-3}\)

These samples were supplied by University of Louvain, Louvain-La-Neuve, Belgium, and were fabricated employing its current SOI fabrication process and facilities.

Maximum transconductance (\(g_{m0}\)) and threshold voltage (\(V_{TH}\)) of all devices were extracted from conventional \(I_{DS} \times V_{GS}\) curves, employing an HP 4145B parameter analyzer. The effective channel length, \(L_{eff}\), of each transistor was calculated from mask dimensions
and $\Delta L = -0.16 \, \mu m$, which has been extracted from the L-intercept linear extrapolation on a $1/g_{m0} \times L$ plot, as illustrated in Fig. 1.

![Image of the $1/g_{m0} \times L$ plot](image)

**Fig. 1:** $1/g_{m0} \times L$ plot for extracting $\Delta L$.

Device nominal and extracted effective values were then used as input parameters for simulating the fabrication process of the actual device structure with SUPREM IV, followed by device electrical behavior simulation with MEDICI. Consistent values between experiment and simulation required minor adjustments in the low field maximum mobility as well as inclusion of lattice heating and carrier ionization effects along with self consistent solution of two-dimensional total energy balance, Poisson and continuity equations. Fig. 2 shows a graph with experimental and simulated plots of $I_{DS} \times V_{DS}$ curves from the 1.0 $\mu m$ long device, whereas Fig. 3 illustrates the corresponding curves obtained for the 2.0 $\mu m$ long device.

![Graph of experimental and simulated $I_{DS} \times V_{DS}$ curves for the 1.0 $\mu m$ long device](image)

**Fig. 2:** Experimental and simulated $I_{DS} \times V_{DS}$ curves for the 1.0 $\mu m$ long device.

![Graph of experimental and simulated $I_{DS} \times V_{DS}$ curves for the 2.0 $\mu m$ long device](image)

**Fig. 3:** Experimental and simulated $I_{DS} \times V_{DS}$ curves for the 2.0 $\mu m$ long device.

Notice the negative channel differential conductance in the high $V_{GS}$ curves, characteristic on
both devices. The fitting between simulated and experimental data points are also noticeable, indicating the effectiveness of simulating FD SOI devices by MEDICI and SUPREM IV. Figures 2 and 3 also include the MEDICI $I_{DS} \times V_{DS}$ simulated curves without employing the lattice heating effect. No negative differential channel conductance is observed. Therefore, the latter results would be equivalent to the theoretical electrical behavior of these devices as if no heat would have been generated in the crystal lattice. Experimental evidence of this behavior has been published in the literature [8]. Special techniques that require specific equipment, such as transmission-line circuitry and a narrow-pulse or high-frequency system must be used in order to avoid self-heating during device testing. If the pulse duration is much lower than the SOI structure thermal time constant (about 1 µs, in most cases), no significant heating is achieved.

Indeed, preliminary results, obtained from applying a narrow-pulse (about 20 ns wide, 1 ms period, 6V amplitude) to the gate and a static value, $V_{DS} = 6V$, show that the heating-free $I_{DS} \times V_{DS}$ theoretical behavior can be effectively observed and measured. For instance, in one particular experiment, we have obtained an $I_{DS}$ about 30% higher in the narrow pulse test than that obtained under static operation with similar bias conditions.

3. CONCLUSION

The negative channel output conductance of a FD SOI NMOS device can be simulated by MEDICI, employing the lattice heating module, as long as suitable structure geometry and doping parameters are utilized to produce experimental and simulated results with a remarkable good fit. The results also indicate that both, self-heating free simulated and narrow pulse tested experimental values for $I_{DS}$ are up to 30% higher than their static counterparts when pulsed $V_{GS}$ and static $V_{DS}$ equal 6V are applied to the device terminals.

4. ACKNOWLEDGMENTS

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5. REFERENCES