Abstract

The influence of “in situ” wafer cleaning process has been studied in the quality of TEOS-PECVD silicon oxide deposited in a home made cluster tool system. We used MOS capacitor structure with and without polysilicon layer to perform the C-V measurements. The results showed that “in situ” cleaning process cause damages in the silicon surfaces.

Introduction

Deposition of silicon dioxide films at low temperature by the Plasma Enhanced Chemical Vapor Deposition (PECVD) has large applications on silicon integrated circuits technology.[1-4]

Silicon oxide deposition from tetraethylorthosilicate (TEOS) provides excellent conformality, which is not achievable when silane is used as silicon source.[5] Nevertheless, poor electrical characteristics is reported for silicon oxide films deposited by TEOS-PECVD; due to the problems related with process parameters control as pressure, temperature, TEOS/O\textsubscript{2} ratio, etc.[6-8]. Also, the Si/SiO\textsubscript{2} interface plays a role in the electrical behavior of SiO\textsubscript{2} films[3,7]. To improve the interface Si/SiO\textsubscript{2} quality, we used two “in situ” cleaning process before the TEOS silicon oxide deposition.

This paper shows the influence of these cleaning process in the electrical behavior of MOS capacitors.

Experimental

Silicon substrates used for TEOS PECVD oxide deposition were 51 mm, n-type <100>; 1-20 Ω.cm. Figure 1 shows the MOS capacitors structures used in this experiment.

![Figure 1: Capacitors structures used in this experiment.](image-url)
It was used the follows wafer cleaning processes:

- Normal - conventional RCA cleaning.
- CF$_4$+O$_2$ - “in situ” cleaning process using CF$_4$-O$_2$ plasma in the following conditions: 100 sccm CF$_4$, 20 sccm O$_2$, work pressure 0.5 Torr, RF Power 100 W during 1 min.
- O$_2$ - “in situ” treatment of the silicon substrate using O$_2$ plasma in the following conditions: 20 sccm O$_2$, work pressure 0.5 Torr, RF Power 100 W during 1 min.

Table I shows the deposition process parameters used in TEOS-PECVD silicon oxide deposition carried out in a home made cluster tool system\textsuperscript{[4]}.

<table>
<thead>
<tr>
<th>Table I: Deposition process parameters used for TEOS PECVD silicon oxide deposition.</th>
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</thead>
<tbody>
<tr>
<td>RF power (W)</td>
</tr>
<tr>
<td>Temperature (°C)</td>
</tr>
<tr>
<td>Distance between electrodes (mm)</td>
</tr>
<tr>
<td>Oxygen flux (sccm)</td>
</tr>
<tr>
<td>TEOS flux (sccm)</td>
</tr>
<tr>
<td>Process pressure (Torr)</td>
</tr>
<tr>
<td>Thickness (nm)</td>
</tr>
</tbody>
</table>

The TEOS PECVD silicon oxide thickness and refractive index measurements were made in a Rudolph Research ellipsometer model Auto-El-NIR3.

Before TEOS PECVD deposition process, it was made a chamber wall cleaning process using a plasma of a mixture of 100 sccm CF$_4$ and 20 sccm O$_2$. This procedure ensures the same initial conditions for all deposition process.

The process for polysilicon was carried out in a home made LPCVD (Low Pressure CVD) system initially in the following conditions: work pressure 1.5 Torr, 50 sccm SiH$_4$, 550°C, deposition rate of 5 nm/s to have an amorphous film. After the deposition process, the amorphous thin film was annealed in the same furnace, during 12 hs at 600°C in vacuum, to obtain a polycrystalline layer. To remove the polysilicon layer from the backside of the wafer a SF$_6$ plasma etching process has been performed in the following conditions 20 sccm SF$_6$, 30 mTorr, 50 W, 1 min.

The evaporated Aluminum thin film had ~300 nm thick. The MOS capacitors (area=2.25 µm$^2$) was patterned by conventional lithography process. Capacitance Voltage-High Frequency (CV-HF) measurements were performed in a HP CV-4140 analysis station.
Results and Discussion

Figure 2 shows the CV-HF curves obtained from the capacitors structures.

Figure 2: CV-HF curves from SiO₂-TEOS/Al and SiO₂-TEOS/Si-poli/Al structures
Table II shows the electrical parameters ($C_{fb}$-Flat Band Capacitance, $V_{fb}$-Flat Band Voltage and $N_{ss}$-interface charge density), calculated from the CV-HF curves.

<table>
<thead>
<tr>
<th>Surface preparation</th>
<th>Sample</th>
<th>SiO$_2$ thickness measured (nm)</th>
<th>Refractive Index</th>
<th>$C_{fb}$ (pF)</th>
<th>$N_{ss}$ (charge/cm$^2$)</th>
<th>$V_{fb}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>F1(poly)</td>
<td>65.9</td>
<td>1.490</td>
<td>4.90</td>
<td>3.11E09</td>
<td>-0.2</td>
</tr>
<tr>
<td></td>
<td>F3(Al)</td>
<td>56.1</td>
<td>1.497</td>
<td>5.97</td>
<td>1.49E11</td>
<td>0.5</td>
</tr>
<tr>
<td>CF$_4$+O$_2$</td>
<td>F4(poly)</td>
<td>45.4</td>
<td>1.504</td>
<td>8.65</td>
<td>1.09E11</td>
<td>-1</td>
</tr>
<tr>
<td></td>
<td>F6(Al)</td>
<td>46.4</td>
<td>1.478</td>
<td>9.90</td>
<td>1.89E11</td>
<td>0.2</td>
</tr>
<tr>
<td>O$_2$</td>
<td>F7(poly)</td>
<td>65.1</td>
<td>1.453</td>
<td>5.45</td>
<td>1.19E11</td>
<td>-0.9</td>
</tr>
<tr>
<td></td>
<td>F9(Al)</td>
<td>49.1</td>
<td>1.469</td>
<td>9.84</td>
<td>4.76E11</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Figure 3 shows a histogram comparing the $N_{ss}$ values for each wafer cleaning procedure. The highest $N_{ss}$ value was obtained for sample F9, that was treated with “in situ” O$_2$ plasma. The Al/SiO$_2$ structure showed higher $N_{ss}$ values compared with SiO$_2$/Poly/Al.

![Figure 3: Histogram comparing the Nss values obtained for each wafer cleaning procedure.](image)

The results observed in figure 3 related to the differences between capacitors structures can be attributed to the two thermal steps which the SiO$_2$ films were submitted during polysilicon deposition.

SiO$_2$ films deposited by CVD and submitted to thermal treatment for several hours can bear modifications on the film structure and composition and consequently the electrical behavior of these films are changed $^{[4,7,9]}$ also when TEOS is used as a Si precursor, some radicals like Si-OH and C-O can be incorporated into the film bulk.$^{[10]}$
Thermal processes can either eliminate the Si-OH and C-O radicals that are trapped in the film during TEOS-PECVD SiO$_2$ deposition process and/or modify the SiO$_2$ structure. However, this process depends on temperature, time of thermal treatment and on radical nature. These mechanisms still not well understood$^{[9-11]}$.

We can conclude that the lower $N_{ss}$ value obtained for the polysilicon capacitors should be due to the thermal steps during LPCVD polysilicon deposition process.

The quality and/or the condition of the silicon wafer surface can influence the deposition process and the oxide quality.$^{[3,7]}$

Silicon wafer cleaned with conventional RCA process with final dip in HF solution, presents mainly Si-H on the surface. This surface can improve the nucleation sites of the deposition process and can lower the interface charges$^{[12]}$.

O$_2$ plasma is used before the PECVD-TEOS SiO$_2$ deposition, to grow a thin oxide layer over the wafer surface. In this case, we can improve the quality of the interface Si/SiO$_2$. However, we also increase the density of the impurities damage in the Si/SiO$_2$ interface. In our case these impurities increased the $N_{ss}$ values as observed in the figure 3.$^{[3,8]}$

A CF$_4$-O$_2$ plasma treatment could reduce the influence of the native oxide producing a “cleaner” surface. However, CF$_4$ plasma also produce organic polymers which can be deposited over the silicon wafer. These residues act as electrical charges in the Si/SiO$_2$ interface.

Plasma treatments performed over silicon wafer surfaces can also increase the roughness by ions bombardments , which agrees with the results.$^{[13]}$

**Conclusions**

We showed that the SiO$_2$ film structure and electrical behavior are modified by thermal treatments. The thermal steps used during the polysilicon deposition, improve the electrical behavior of the SiO$_2$-TEOS films

The silicon wafer surface quality is influenced by the cleaning treatment that are performed before SiO$_2$ films deposition.

We report that the regular chemical cleaning process (RCA) is better than the “in situ” plasma treatments

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References


